

I CLAIM:

1. Apparatus for processing data, said apparatus comprising:

5 a processor operable to perform data processing operations under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and

10 a mapping circuit operable to map said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level.

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2. Apparatus as claimed in claim 1, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency, said clock signal being supplied to said processor to drive said processing operations such that data processing performance of said processor varies in dependence upon which clock frequency is selected.

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3. Apparatus as claimed in claim 1, wherein said one or more further circuits include a voltage controller operable to generate a power supply signal, said power supply signal being supplied to said processor at a selectable voltage level, different voltage levels allowing different switching speeds within said processor such that a maximum usable data processing performance varies in dependence upon which voltage level is selected.

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4. Apparatus as claimed in claim 1, wherein said control signal is a thermometer coded value.

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5. Apparatus as claimed in claim 4, having a plurality of processors and mapping circuits operable to generate respective thermometer coded values which are logically

combined to produce a combined thermometer coded value to control at least one of said one or more further circuits.

6. Apparatus as claimed in claim 1, wherein said mapping circuit performs a
5 many to one mapping between performance level request signal values and
corresponding control signal values.

7. Apparatus as claimed in claim 6, wherein said control signals are quantised
such that a control signal value supports a maximum desired performance level within
10 a range of desired performance levels having corresponding performance level request
signal values mapped to said control signal value.

8. Apparatus as claimed in claim 1, wherein performance level supported as
controlled by control signal value increases monotonically with performance level
15 request signal value.

9. Apparatus as claimed in claim 1, wherein at least one of said one or more
further circuits operates in a different clock domain to said processor.

20 10. Apparatus as claimed in claim 1, wherein at least one of said one or more
further circuits is configured with one or more configuration values specifying how
said further circuit should respond to different control signal values.

11. Apparatus as claimed in claim 3, wherein said configuration values specify
25 voltage levels corresponding to different control signal values.

12. Apparatus as claimed in claim 1, wherein while responding to a change in
performance control signal corresponding to a change from a first desired data
processing performance level to a second desired data processing performance level,
30 said one or more further circuits are operable to support data processing at at least one
intermediate data processing performance level and said processor temporarily
operates at said at least one intermediate data processing performance level during
said change.

13. Apparatus as claimed in claim 2, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency.

14. Apparatus as claimed in claim 12, wherein a priority signal serves to trigger said further circuit to change to support a predetermined data processing performance level independently of said performance control signal.

10 15. Apparatus as claimed in claim 1, wherein at least while responding to a change in said performance control signal, said further circuit is operable to generate a current operation signal indicative of current operation of said further circuit.

15 16. Apparatus as claimed in claim 3, wherein said current operation signal is indicative of a maximum power supply voltage of that can currently be supported by said voltage controller.

17. Apparatus as claimed in claim 2, wherein said currently operation signal is indicative of a clock frequency that is currently being generated by said clock generator.

20 18. Apparatus as claimed in claim 2, wherein said clock generator is operable to generate a clock signal with one or more permanently available clock signal frequencies and one or more selectively available clock signal frequencies.

25 19. Apparatus as claimed in claim 18, wherein a permanently enabled PLL circuit is operable to generate said one or more permanently available clock signal frequencies and a selectively enabled PLL circuit is operable to generate said one or more selectively available clock signal frequencies.

30 20. Apparatus as claimed in claim 16, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency when said voltage controller generates a current operation signal indicative

of a generation of said power signal with a voltage level sufficient to support an increased clock signal frequency.

21. A method of processing data, said method comprising the steps of:

5 performing data processing operations with a processor under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and

10 mapping with a mapping circuit said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level.

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22. A method as claimed in claim 21, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency, said clock signal being supplied to said processor to drive said processing operations such that data processing performance of said processor varies in 20 dependence upon which clock frequency is selected.

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23. A method as claimed in claim 21, wherein said one or more further circuits include a voltage controller operable to generate a power supply signal, said power supply signal being supplied to said processor at a selectable voltage level, different 25 voltage levels allowing different switching speeds within said processor such that a maximum usable data processing performance varies in dependence upon which voltage level is selected.

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24. A method as claimed in claim 21, wherein said control signal is a thermometer 30 coded value.

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25. A method as claimed in claim 24, wherein a plurality of processors and mapping circuits generate respective thermometer coded values which are logically

combined to produce a combined thermometer coded value to control at least one of said one or more further circuits.

26. A method as claimed in claim 21, wherein said mapping is a many to one
5 mapping between performance level request signal values and corresponding control signal values.

27. A method as claimed in claim 26, wherein said control signals are quantised such that a control signal value supports a maximum desired performance level within
10 a range of desired performance levels having corresponding performance level request signal values mapped to said control signal value.

28. A method as claimed in claim 21, wherein performance level supported as controlled by control signal value increases monotonically with performance level
15 request signal value.

29. A method as claimed in claim 21, wherein at least one of said one or more further circuits operates in a different clock domain to said processor.

20 30. A method as claimed in claim 21, wherein at least one of said one or more further circuits is configured with one or more configuration values specifying how said further circuit should respond to different control signal values.

31. A method as claimed in claim 23, wherein said configuration values specify
25 voltage levels corresponding to different control signal values.

32. A method as claimed in claim 21, wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level,
30 said one or more further circuits are operable to support data processing at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change.

33. A method as claimed in claim 22, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate

5 clock signal frequency.

34. A method as claimed in claim 32, wherein a priority signal serves to trigger said further circuit to change to support a predetermined data processing performance level independently of said performance control signal.

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35. A method as claimed in claim 21, wherein at least while responding to a change in said performance control signal, said further circuit is operable to generate a current operation signal indicative of current operation of said further circuit.

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36. A method as claimed in claim 23, wherein said current operation signal is indicative of a maximum power supply voltage of that can currently be supported by said voltage controller.

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37. A method as claimed in claim 22, wherein said currently operation signal is indicative of a clock frequency that is currently being generated by said clock generator.

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38. A method as claimed in claim 22, wherein said clock generator is operable to generate a clock signal with one or more permanently available clock signal frequencies and one or more selectively available clock signal frequencies.

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39. A method as claimed in claim 38, wherein a permanently enabled PLL circuit is operable to generate said one or more permanently available clock signal frequencies and a selectively enabled PLL circuit is operable to generate said one or more selectively available clock signal frequencies.

40. A method as claimed in claim 36, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency when said voltage controller generates a current operation signal indicative

of a generation of said power signal with a voltage level sufficient to support an increased clock signal frequency.

41. A computer program product containing program instructions for controlling a
5 processor to operate in accordance with the method as claimed in claim 22.

42. A computer program product containing program instructions for controlling a
processor, said program instructions comprising:

10 program instructions executable by said processor to set a desired data
processing performance level to control one or more further circuits to support said
desired data processing performance level operate, said desired data processing
performance level having value linearly related to said desired data processing
performance level.

15 43. A computer program product as claimed in claim 42, wherein said desired data
processing performance level has a value equivalent to a binary fraction of a
maximum data processing performance level.